# Engineering Specification

## Type 15.0 XGA Color TFT/LCD Module
## Model Name:N150X4-L01

## Document Control Number : OEM N150X4-L01-01

**Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.**

**Sales Support**
**International Display Technology**

# i Contents

## ii  Record of Revision

| Date | Document Revision | Page | Summary |
|------|-------------------|------|---------|
| February 06,2003 | OEM N150X4-L01-01 | All | First Edition for customer. Based on Internal Spec."N150X4-IPI-01" |

## 1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.

- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.

- CMOS ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.

- Do not press the reflector sheet at the LCD module to any directions.

- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.

- Please handle with care when mount in the system cover. Mechanical damage for lamp cable/lamp connector may cause safety problems.

- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.

- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950).

- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.

-  Never apply detergent or other liquid directly to the screen.

- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use  solvents or abrasives.

- Do not touch the front screen surface in your system, even bezel.

- Gently wipe the covers and the screen with a soft cloth.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

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## 2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'N150X4-L01'.
This module is designed for a display unit of a notebook style personal computer.
The screen format and electrical interface are intended to support the XGA (1024(H) x 768(V)) screen.
Support color is native 262k colors ( RGB 6-bit data driver ).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

## 2.1  Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

| CHARACTERISTICS ITEMS | SPECIFICATIONS |
|---|---|
| Screen Diagonal  [cm] | 38 |
| Active Area  [mm] | 304.128(H) x 228.096(V) |
| Pixels H x V [pixels] | 1024(x3) x 768 |
| Pixel Pitch  [mm] | 0.297(per one triad) x 0.297 |
| Pixel Arrangement | R.G.B. Vertical Stripe |
| Display Mode | Normally Black |
| White Luminance  [cd/m$^2$] | 215 Typ. (Screen Center, ICFL = 6.5mA) |
| Contrast Ratio | 400 : 1 Typ. 300:1 Min |
| Viewing Angle | CR>=10:1    H: +/-85 deg., V:+/-85 deg. Typ.<br>CR>=100:1   H: +/-40 deg., V:+/-40 deg. Typ. |
| Color Chromaticity | x:0.313 , y:0.329 |
| Surface Treatment | Anti-Glare,AG160 |
| Optical Rise + Fall Time | 60msec Typ.;   120ms Max. (@25degC) |
| Nominal Input Voltage  [VDD] | +3.3  V |
| Logic Power Consumption  [watt] | 1.6 Typ. (All White Pattern), 2.2 Max (worst pattern) |
| CFL Power Consumption  [watt] | 4.1Typ.(@ICFL=6.5mA) |
| Weight  [grams] | 585 Max. |
| Physical Size  [mm] | 317.3(W) x 242.0(H) x 6.2(D) Typ. |
| Electrical Interface | 4 pairs Single LVDS(Single) |
| Support Color | Native 262K colors ( RGB 6-bit data driver ) |
| Temperature Range [deg. C] | 0 to +50 (Operating)<br>-20 to +60 (Storage, Shipping) |
| CFL cable length | 60 mm |

## 2.2  Functional Block Diagram

The  following diagram shows the functional block of the Type 15.0 Color TFT/LCD Module.
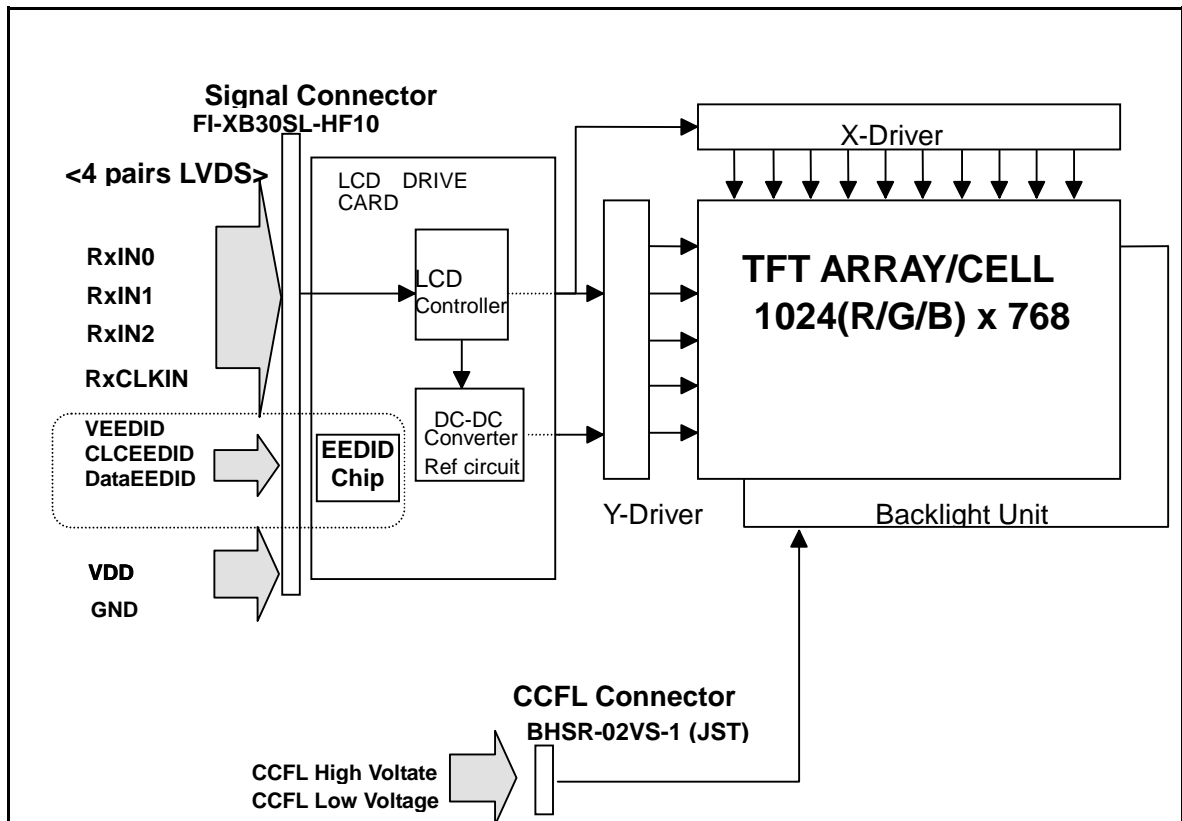
# 3.0  Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

| Item | Symbol | Min | Max | Unit | Conditions |
|------|--------|-----|-----|------|------------|
| Supply Voltage | VDD | -0.3 | +4.0 | V | |
| Input Voltage of Signal | Other Inputs | -0.3 | VDD+0.3 | V | |
| Lamp Ignition Voltage | Vinv | - | 2,000 | Vrms | |
| CFL Current | ICFL | - | 7 | mArms | |
| CFL Peak Inrush Current | ICFLP | - | 20mA / 50ms | | A single pulse |
| Operating Temperature | TOP | 0 | +50 | deg.C | **(Note 1)** |
| Operating Relative Humidity | HOP | 8 | 95 | %RH | **(Note 1)** |
| Storage Temperature | TST | -20 | +60 | deg.C | **(Note 1)** |
| Storage Relative Humidity | HST | 5 | 95 | %RH | **(Note 1)** |
| Vibration | | | 1.5    10-200 | G    Hz | |
| Shock | | | 50    18 | G    ms | Rectangle wave |

**Note :**
1.  Maximum Wet-Bulb should be 39 degree C and No condensation.

# 4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

| Item | Conditions | | Specification | |
|---|---|---|---|---|
| | | | Typ. | Note |
| Viewing Angle (Degrees) | Horizontal (Right) K≥10 (Left) | | 85 85 | - - |
| K:Contrast Ratio | Vertical (Upper) K≥10 (Lower) | | 85 85 | - - |
| Contrast ratio | | | 400 | - |
| Response Time (ms) | Rising + Falling | | 60 | 120 Max. |
| Color | Red x | | - | - |
| Chromaticity | Red y | | - | - |
| (CIE) | Green x | | - | - |
| | Green y | | - | - |
| | Blue x | | - | - |
| | Blue y | | - | - |
| | White x | | 0.313 | - |
| | White y | | 0.329 | - |
| White Luminance (cd/m$^2$) ICFL 6.0 mA | | | 200Typ. Center | 160Min Center |

# 5.0 Signal Interface

## 5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|---|---|
| Manufacturer | JAE |
| Type / Part Number | FI-XB30SL-HF10 |
| Mating Receptacle/Part Number | FI-X30M, FI-X30C2L |

| Connector Name / Designation | For Lamp Connector |
|---|---|
| Manufacturer | JST |
| Type / Part Number | BHSR-02VS-1 |
| Mating Type / Part Number | SM02B-BHSS-1 |

## 5.2 Interface Signal Connector

| Pin # | Signal Name | | Pin # | Signal Name |
|-------|-------------|---|-------|-------------|
| 1 | GND | | 16 | GND |
| 2 | VDD | | 17 | RxCLKIN- |
| 3 | VDD | | 18 | RxCLKIN+ |
| 4 | V$_{EDID}$ **(Note 2, 3)** | | 19 | GND |
| 5 | Reserved **(Note 1)** | | 20 | NC |
| 6 | CLK$_{EEDID}$ **(Note 2, 4)** | | 21 | NC |
| 7 | Data$_{EEDID}$ **(Note 2, 4)** | | 22 | GND |
| 8 | RxIN0- | | 23 | NC |
| 9 | RxIN0+ | | 24 | NC |
| 10 | GND | | 25 | GND |
| 11 | RxIN1- | | 26 | NC |
| 12 | RxIN1+ | | 27 | NC |
| 13 | GND | | 28 | GND |
| 14 | RxIN2- | | 29 | NC |
| 15 | RxIN2+ | | 30 | NC |

**Note :**
1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3".
3. V$_{EEDID}$ power source shall be the limited current circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC™) Proposed Standard", VESA)
4. Both CLK$_{EEDID}$ line and DATA$_{EEDID}$ line are pulled up with 10k ohm resistor to V$_{EEDID}$ power source line at LCD panel, respectively.

   Voltage levels of all input signals are LVDS compatible (except VDD, EEDID). Refer to "Signal Electrical Characteristics for LVDS Receiver", for voltage levels of all input signals.

## 5.3 Interface Signal Description

Signal Description

| Signal Name | Description |
|-------------|-------------|
| RxIN0+, RxIN0- | LVDS differential data input (Red0-Red5, Green0) |
| RxIN1+, RxIN1- | LVDS differential data input (Green1-Green5,Blue0-Blue1) |
| RxIN2+, RxIN2- | LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG) |
| RxCLKIN+, RxCLKIN- | LVDS differential clock input |
| VDD | +3.3V Power Supply |
| GND | Ground |

**Note :**
• Input signals shall be low or Hi-Z state when VDD is off.

| SIGNAL NAME | Description |
|---|---|
| +RED5<br>+RED4<br>+RED3<br>+RED2<br>+RED1<br>+RED0 | Red Data 5 (MSB)<br>Red Data 4<br>Red Data 3<br>Red Data 2<br>Red Data 1<br>Red Data 0 (LSB)<br><br>Red-pixel Data: Each red pixcel's brightness data consists of these 6 bits pixel data. |
| +GREEN 5<br>+GREEN 4<br>+GREEN 3<br>+GREEN 2<br>+GREEN 1<br>+GREEN 0 | Green Data 5 (MSB)<br>Green Data 4<br>Green Data 3<br>Green Data 2<br>Green Data 1<br>Green Data 0 (LSB)<br><br>Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data. |
| +BLUE 5<br>+BLUE 4<br>+BLUE 3<br>+BLUE 2<br>+BLUE 1<br>+BLUE 0 | Blue Data 5 (MSB)<br>Blue Data 4<br>Blue Data 3<br>Blue Data 2<br>Blue Data 1<br>Blue Data 0 (LSB)<br><br>Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data. |
| DTCLK | Data Clock:The typical frequency is 65.0 MHz.<br>The signal is used to strobe the pixel data and the DSPTMG . |
| +DSPTMG(DSP) | When the signal is high, the pixel data shall be valid to be displayed. |
| VSYNC(V-S) | Vertical Sync:The signal is synchronized to DTCLK . Both active high/low signal acceptable. |
| HSYNC(H-S) | Horizontal Sync:The signal is synchronized with DTCLK . Both active high/low signals are acceptable. |
| VDD | Power Supply |
| GND | Ground |
| V$_{EEDID}$ | EEDID 3.3 V Power Supply |
| CLK$_{EEDID}$ | EEDID Clock |
| Data$_{EEDID}$ | EEDID Data |

**Note :** Output signals except V$_{EEDID}$, CLK$_{EEDID}$ and Data$_{EEDID}$ from any system shall be Hi-Z state when VDD is off.

### 5.3.1 E-EDID

E-EDID detail in this LCD module is in the following table.

| Address (hex) | Description | Data (hex) | Remark |
|---|---|---|---|
| 00 - 07 | Header | 00 FF FF FF FF FF FF 00 | Header, Fixed |
| 08 - 09 | ID Manufacturer Name | 24 94 | "IDT" |
| 0A - 0B | ID Product Code | 0D 00 | Product Code |
| 0C - 0F | ID Serial Number | 00 00 00 00 | Unused |
| 10 | Week of Manufacture | 00 | Unused |
| 11 | Year of Manufacture | 00 | Unused |
| 12 - 13 | EDID Structure Version / Revision | 01 03 | Ver1.3 |
| 14 - 18 | Basic Display Parameter / Features | 80 1E 17 78 0A | Active Area : 30.41cm x 22.81cm, Gamma : 2.2 |
| 19 - 22 | Color Characteristics | (Note 1) | |
| 23 - 25 | Established Timing | 00 00 00 | Unused |
| 26 - 35 | Standard Timing Identification | 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 | Unused |
| 36 - 47 | Detailed Timing / Monitor Description #1 | 64 19 00 40 41 00 26 30 18 88 36 00 30 E4 10 00 00 18 | Typical Timing |
| 48 - 59 | Detailed Timing / Monitor Description #2 | (Note 1) | |
| 5A - 6B | Detailed Timing / Monitor Description #3 | 00 00 00 FE 00 49 44 54 0A 20 20 20 20 20 20 20 20 20 | Manufactuerer name "IDT" |
| 6C - 7D | Detailed Timing / Monitor Description #4 | 00 00 00 FE 00 4E 31 35 30 58 34 0A 20 20 20 20 20 20 | Manufacturer P/N "N150X4" |
| 7E | Extension Flag | 00 | No extension |
| 7F | Checksum | (Note 1) | |

Note:

1.Detail data contents shall be determined with concurrence between user and International Display Technology(IDTech).

## 5.4  Interface Signal Electrical Characteristics

### 5.4.1  Signal Electrical Characteristics for LVDS Receiver

The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

Electrical Characteristics

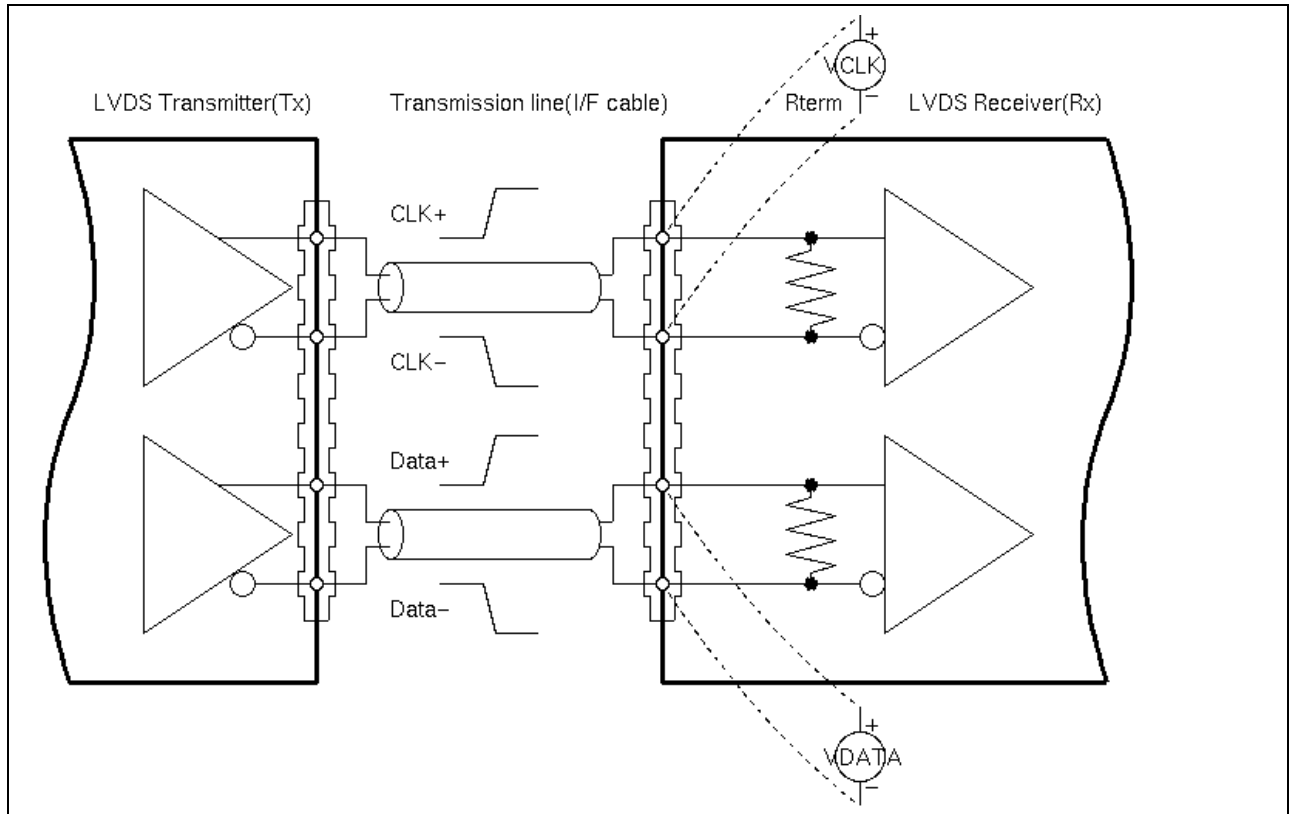| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|-----------|--------|-----|-----|-----|------|------------|
| Differential Input High Threshold | Vth | | | +100 | mV | Vcm=+1.2V |
| Differential Input Low Threshold | Vtl | -100 | | | mV | Vcm=+1.2V |
| Magnitude Differential Input Voltage | \|Vid\| | 100 | | 600 | mV | |
| Common Mode Voltage | Vcm | 1.0 | 1.2 | 1.5 | V | Vth - Vtl = 200mV |
| Common Mode Voltage Offset | △Vcm | -50 | | +50 | mV | Vth - Vtl = 200mV |

**Note :**
- Input signals shall be low or Hi-Z state when VDD is off.

Voltage Definitions
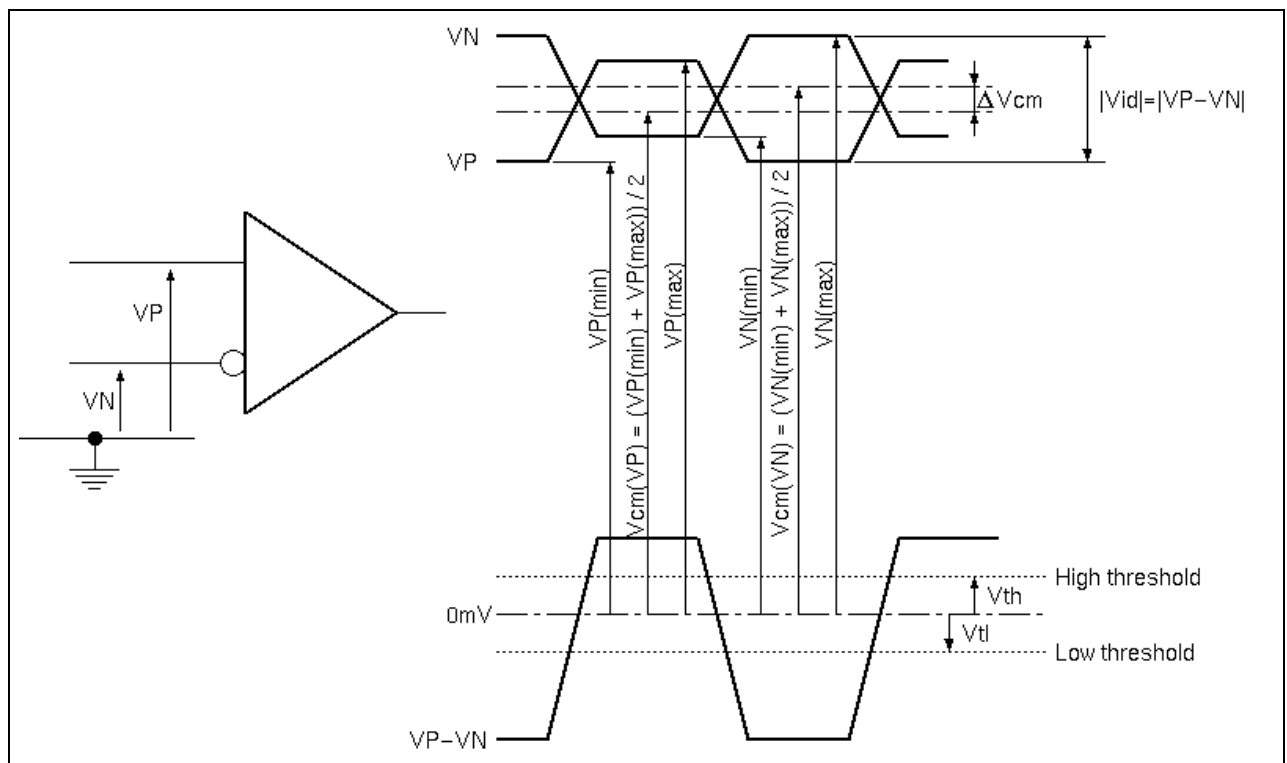
Measurement System



Timming Requirements

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Clock Frequency | fc | 50 | 65 | 67 | MHz | |
| Cycle Time | tc | 14.93 | 15.38 | 20.00 | ns | |
| Data Setup Time (Note 1) | Tsu | 500 | | | ps | fc = 65MHz, tCCJ < 50ps, Vth-Vtl = 400mV, Vcm = 1.2V, △Vcm = 0 |
| Data Hold Time (Note 2) | Thd | 500 | | | ps | |
| Cycle-to-cycle jitter (Note 3) | tCCJ | -150 | | +150 | ps | fc = 65MHz, Tsu=Thd=900ps |
| Cycle Modulation Rate (Note 4) | tCJavg | | | 20 | ps/clk | fc = 65MHz, Tsu=Thd=900ps |

**Note :**
1. All values are at VDD=3.3V, Ta=25 degree C.
2. See figure "**Timing Definition**" and  "**Timing Definition(detail A)**"  for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles.    Figure "**Cycle Modulation Rate**" illustrates a case against this requirement.
   This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.
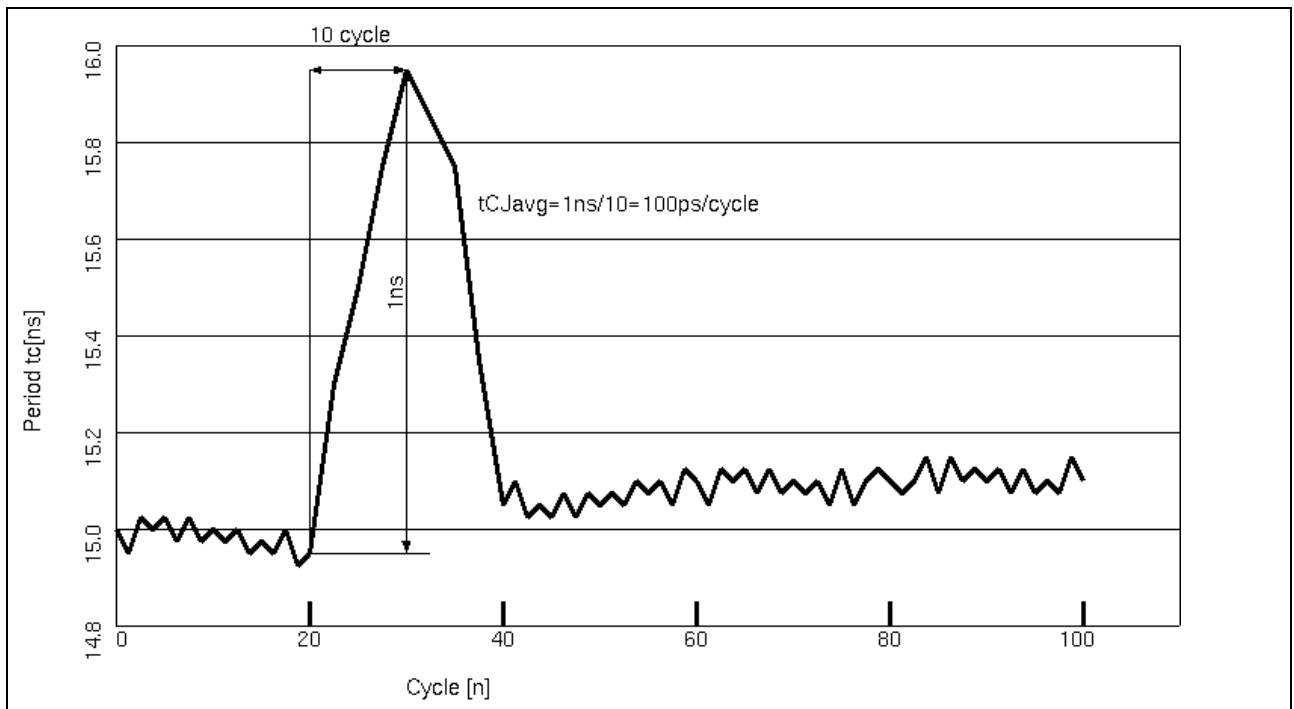
## Timing Definition
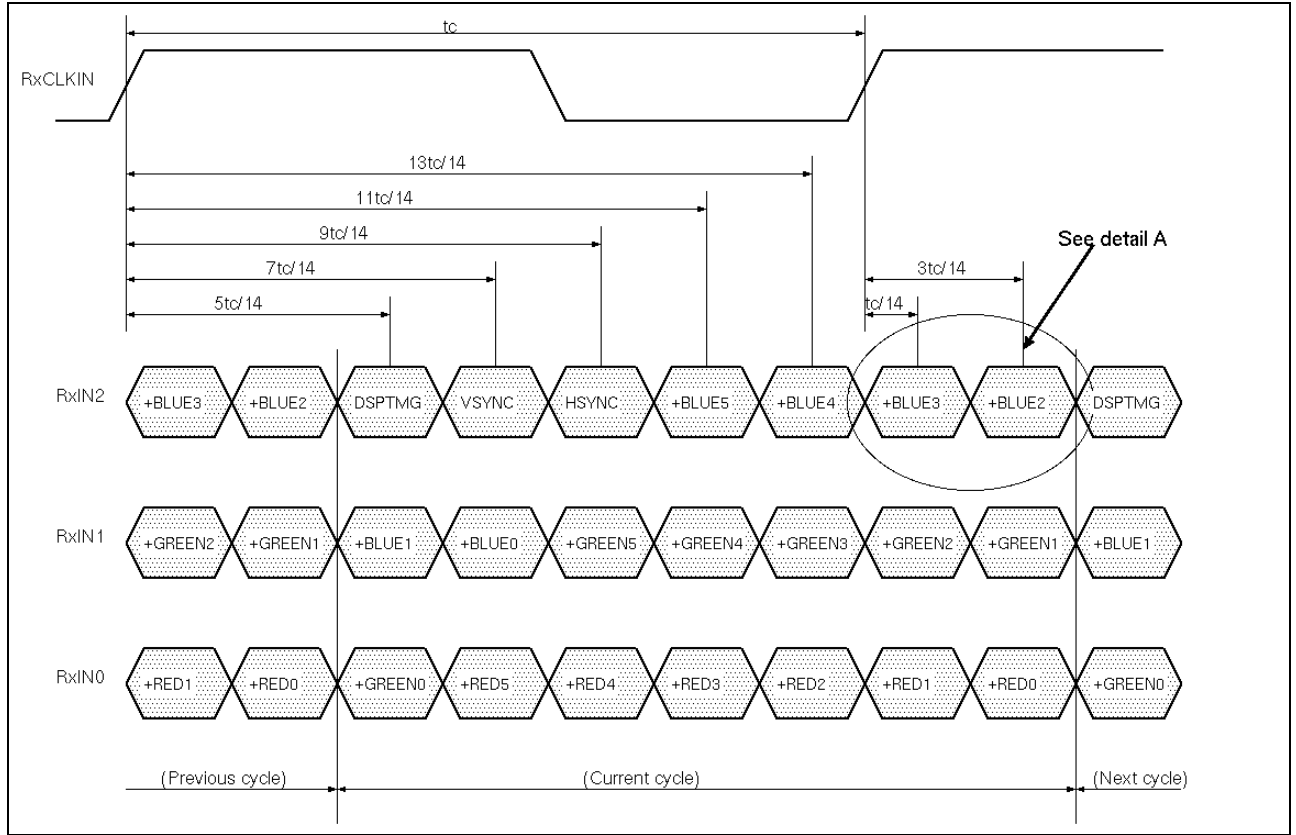
Timing Definition(detail A)
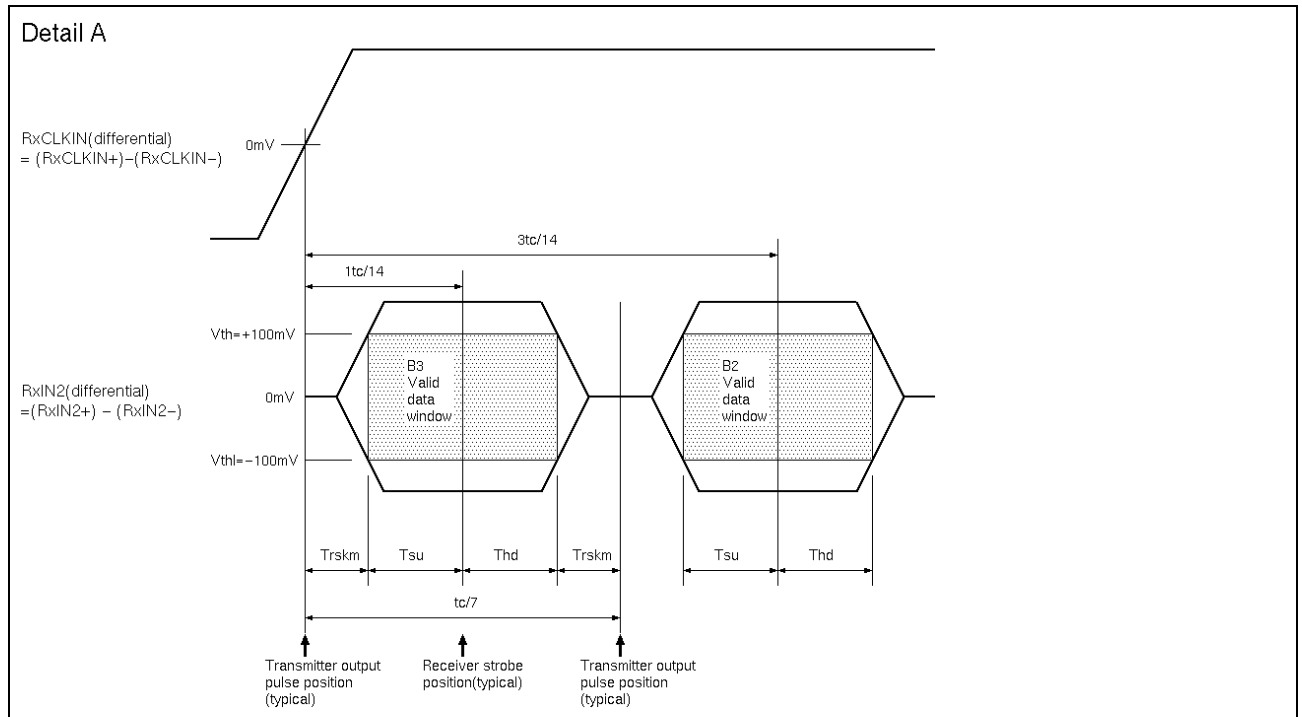


**Note:** Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

Cycle Modulation Rate

### 5.4.2 LVDS Receiver Internal Circuit

The following figure shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.
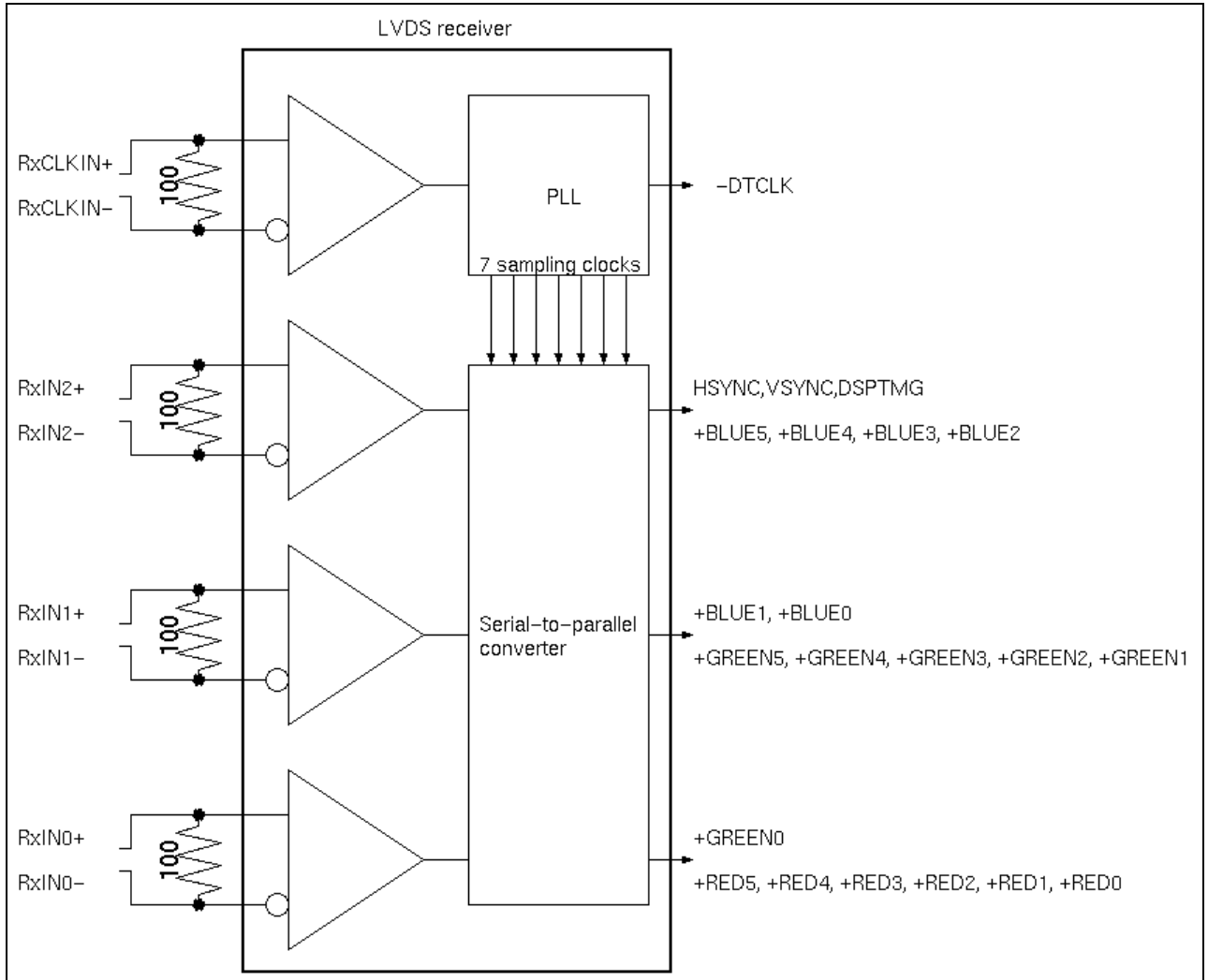


### 5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100 ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twin, or flex circuit with close coupled differential traces are recommended.

## 5.5  Signal for Lamp Connector

| Pin # | Signal Name |
|-------|-------------|
| 1 | Lamp High Voltage |
| 2 | Lamp Low Voltage |

# 6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.
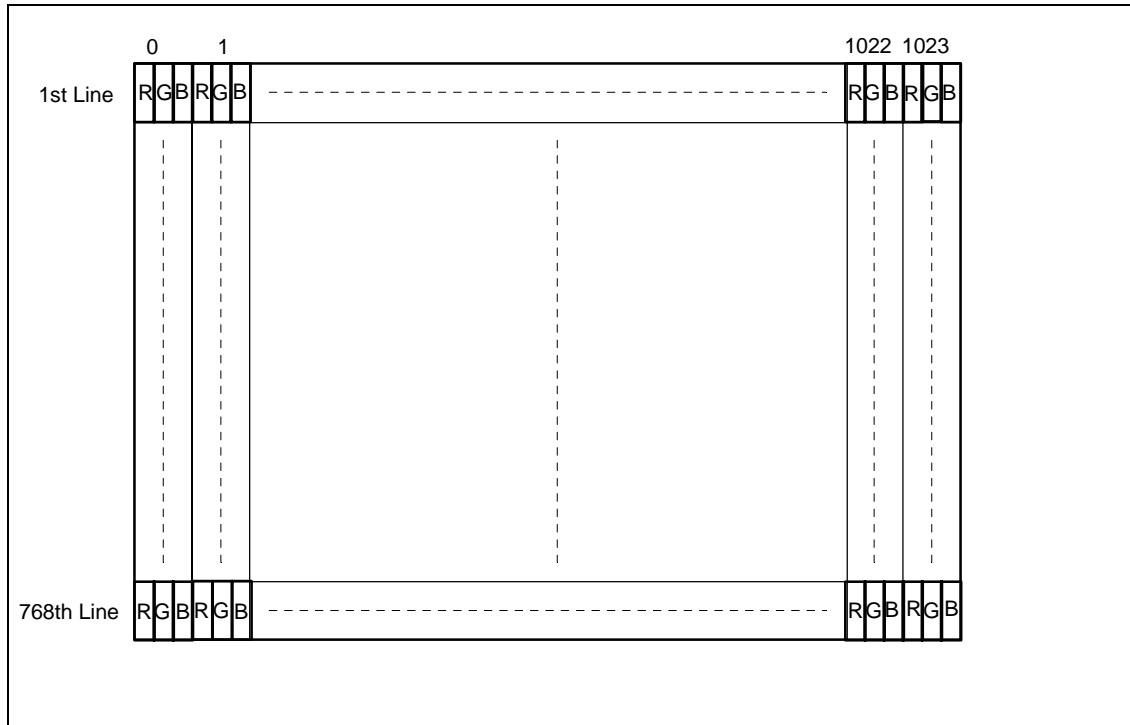
## 7.0 Parameter guide line for CFL Inverter

| SYMBOL | PARAMETER | MIN | D.P (Note 1) | MAX | UNITS | CONDITION |
|--------|-----------|-----|--------------|-----|-------|-----------|
| (L63) | White Luminance (Center) | - - | 215 | - - | [cd/m$^2$] | Ta=25[deg. C] |
| ICFL | CFL current | 3.0 | 6.5 | 7.0 | [mArms] | Ta=25[deg. C] (Note 2,5) |
| ICFLP | CFL Peak Inrush Current | | | 20 | [mA] | Ta=25[deg. C] (Note 2,6) |
| FCFL | CFL Frequency | 40 | | 70 | [kHz] | Ta=25[deg. C] (Note 3) |
| VCFLi | Inverter Ignition Voltage | 1,600 | | | [Vrms] | Ta=0[deg. C] |
| VCFL | CFL Voltage (Reference) | | 630 | | [Vrms] | Ta=25[deg. C] |
| PCFL | CFL Power consumption | | 4.1 | | [W] | Ta=25[deg. C] (Note 4) |

**Note :**
1. Design Point
2. If it exceeds MIN/MAX values, then"CFL Life" , "ON/OFF Cycle", and "SAFETY" will not be guaranteed.
3. CFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD.
4. Calculated value for reference (ICFL x VCFL = PCFL).
5. It should be employed the inverter which has `Duty Dimming`, if ICFL is less than 4[mA].
6. Duration: 50msec MAX

The following chart is Luminance versus Lamp Current for your reference.

TBD
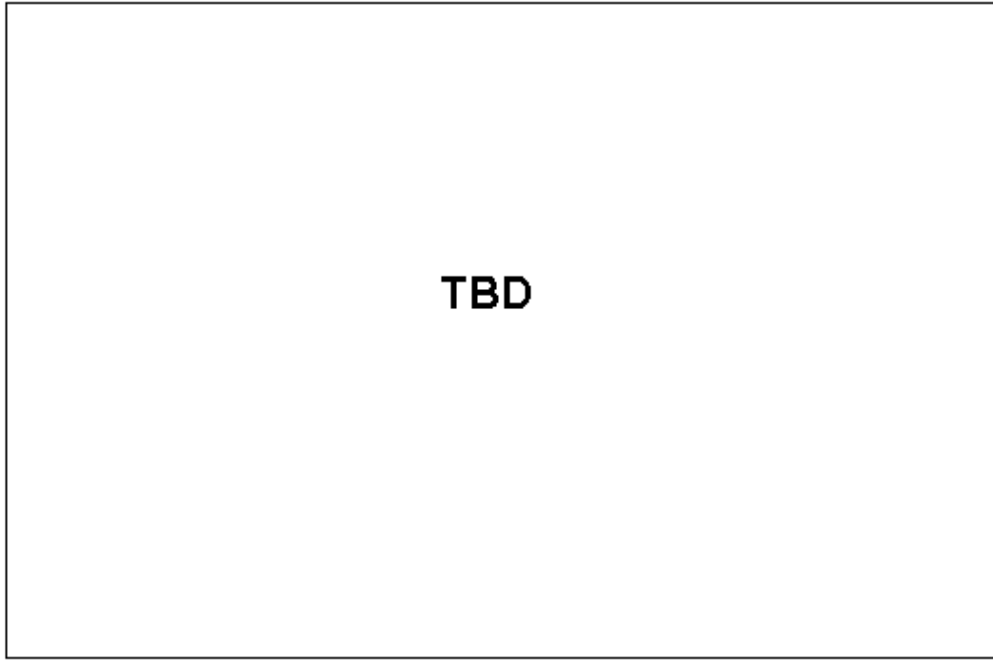
# 8.0  Interface Timings

Basically, interface timings should match the VESA 1024x768 / 60 Hz (VG901101) manufacturing guide line timing. These timings described here are not actual input timings of LCD module but output timings of SN75LVDS86DGG(Texas Instruments) or equivalent.

## 8.1 Timing Characteristics

| Symbol | | MIN | TYP | MAX | Unit | Note |
|--------|------------------|-------|--------|------|------|------|
| fdck   | DTCLK Frequency  | 50.00 | 65.00  | 67.00 | MHz  |      |
| tck    | DTCLK cycle time | 14.93 | 15.38  | 20.00 | nsec |      |
| tx     | X total time     | 1206  | 1344   | 2047 | tck  |      |
| tacx   | X active time    | 1024  | 1024   | 1024 | tck  |      |
| Hsync  | H frequency      |       | 48.363 |      | KHz  |      |
| Hsw    | H-Sync width     | 8     | 136    |      | tck  | 2    |
| Hbp    | H back porch     | 8     | 160    | 510  | tck  | 2    |
| Hfp    | H front porch    | 0     | 24     |      | tck  |      |
| ty     | Y total time     | 777   | 806    | 1023 | tx   |      |
| tacy   | Y active time    | 768   | 768    | 768  | tx   |      |
| Vsync  | Frame rate       | 55    | 60     | 61   | Hz   |      |
| Vw     | V-sync Width     | 1     | 6      |      | tx   |      |
| Vfp    | V-sync front porch | 1   | 3      |      | tx   |      |
| Vbp    | V-sync back porch | 7    | 29     | 63   | tx   | 1    |

**Note1 :** Vbp should be static.
**Note2 :** Hsw+Hbp$\geq$ 32 [tck]

 - The timing interval between V-Sync falling edge and H-Sync rising edge should be fixed between each V-Frame.(V-Sync and H-Sync polarity are assumed to be positive in this case.)

## 8.2 Timing Definition
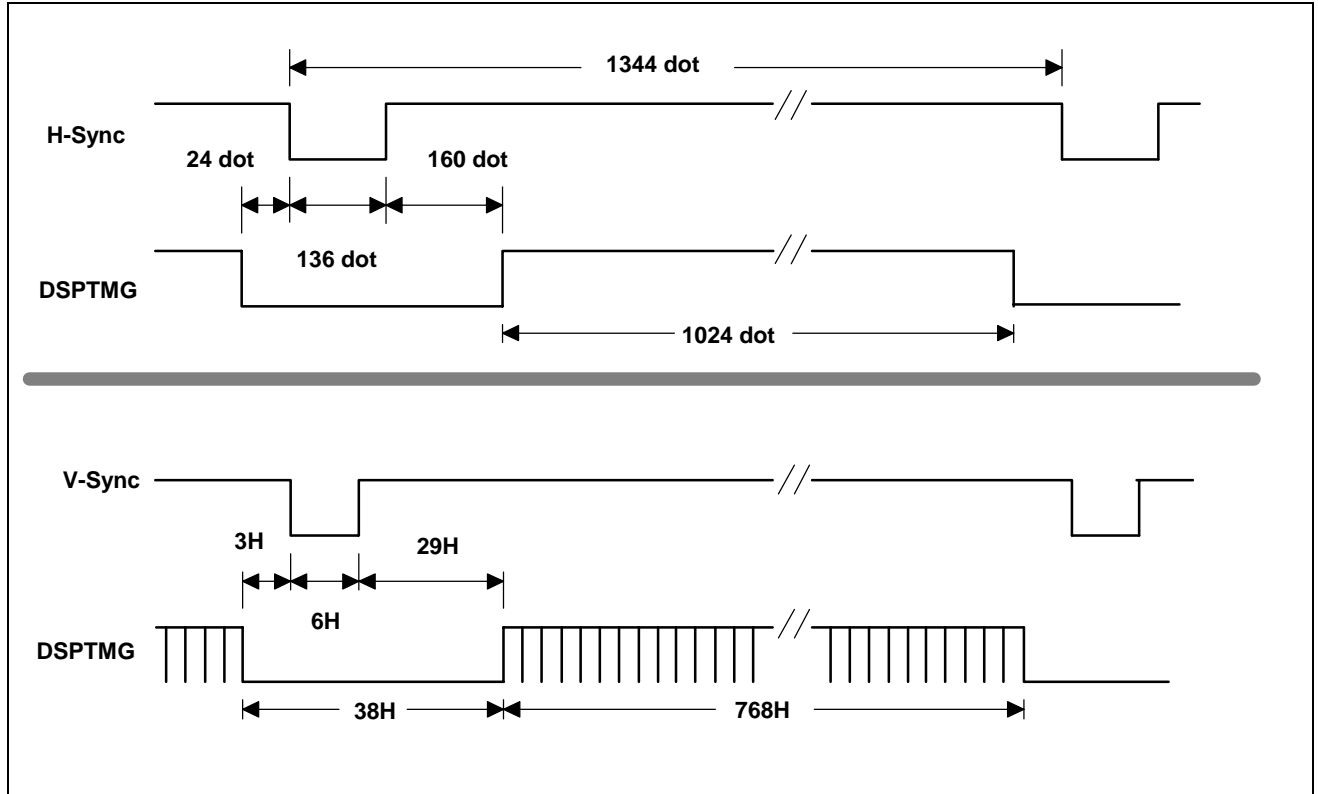
# 9.0  Power Consumption

Input power specifications are as follows;

| SYMBOL | PARAMETER | Min | Typ | Max | UNITS | CONDITION |
|---|---|---|---|---|---|---|
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [V] | Load Capacitance 20[uF] |
| PDD | VDD Power | | 1.6 **(TBD)** | | [W] | All Black Pattern VDD=3.3[V] |
| | | | | 2.2 **(TBD)** | [W] | Max.  Pattern, VDD=3.6[V] |
| IDD | VDD Current | | 490 **(TBD)** | | [mA] | All Black Pattern, VDD=3.3[V] |
| | | | | 640 **(TBD)** | [mA] | Max Pattern, VDD=3.0[V] |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | | | 100 | [mVp-p] | |

## 10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.
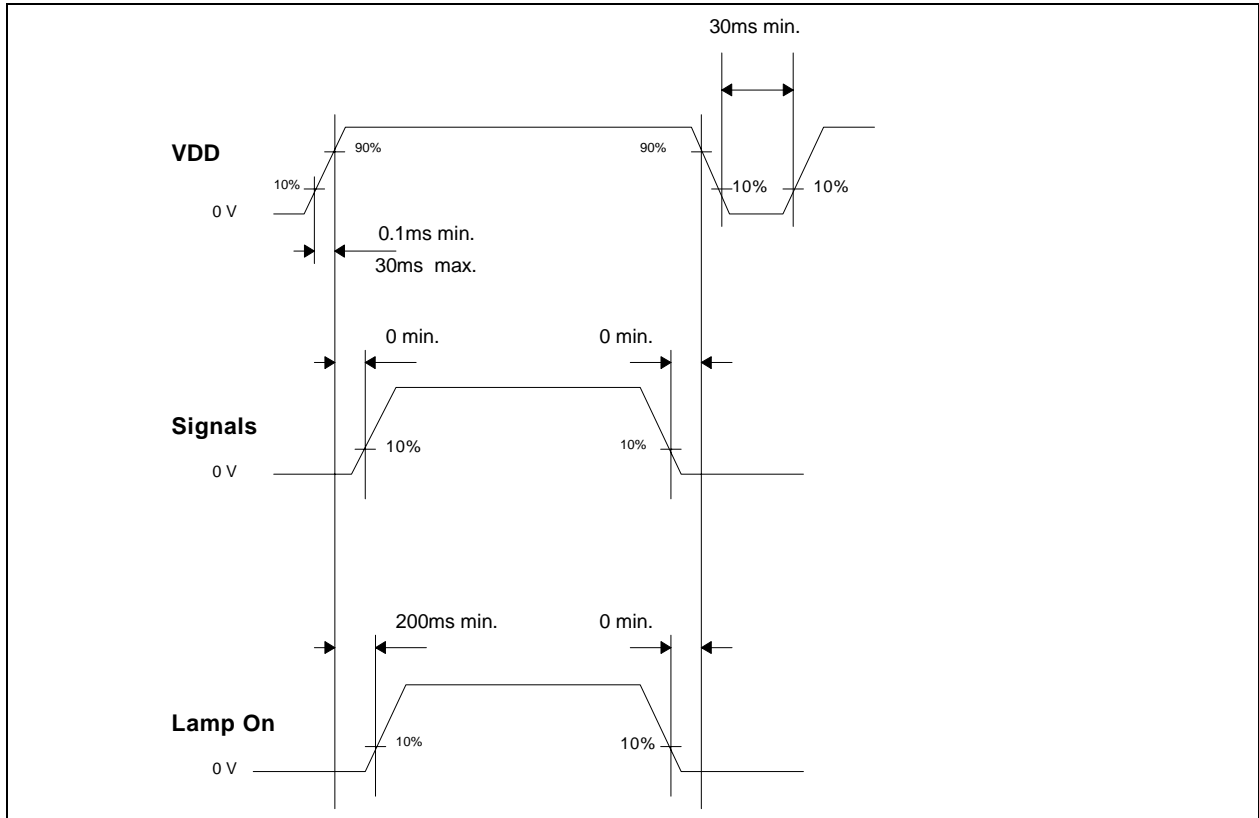
## 11.0  Mechanical Characteristics
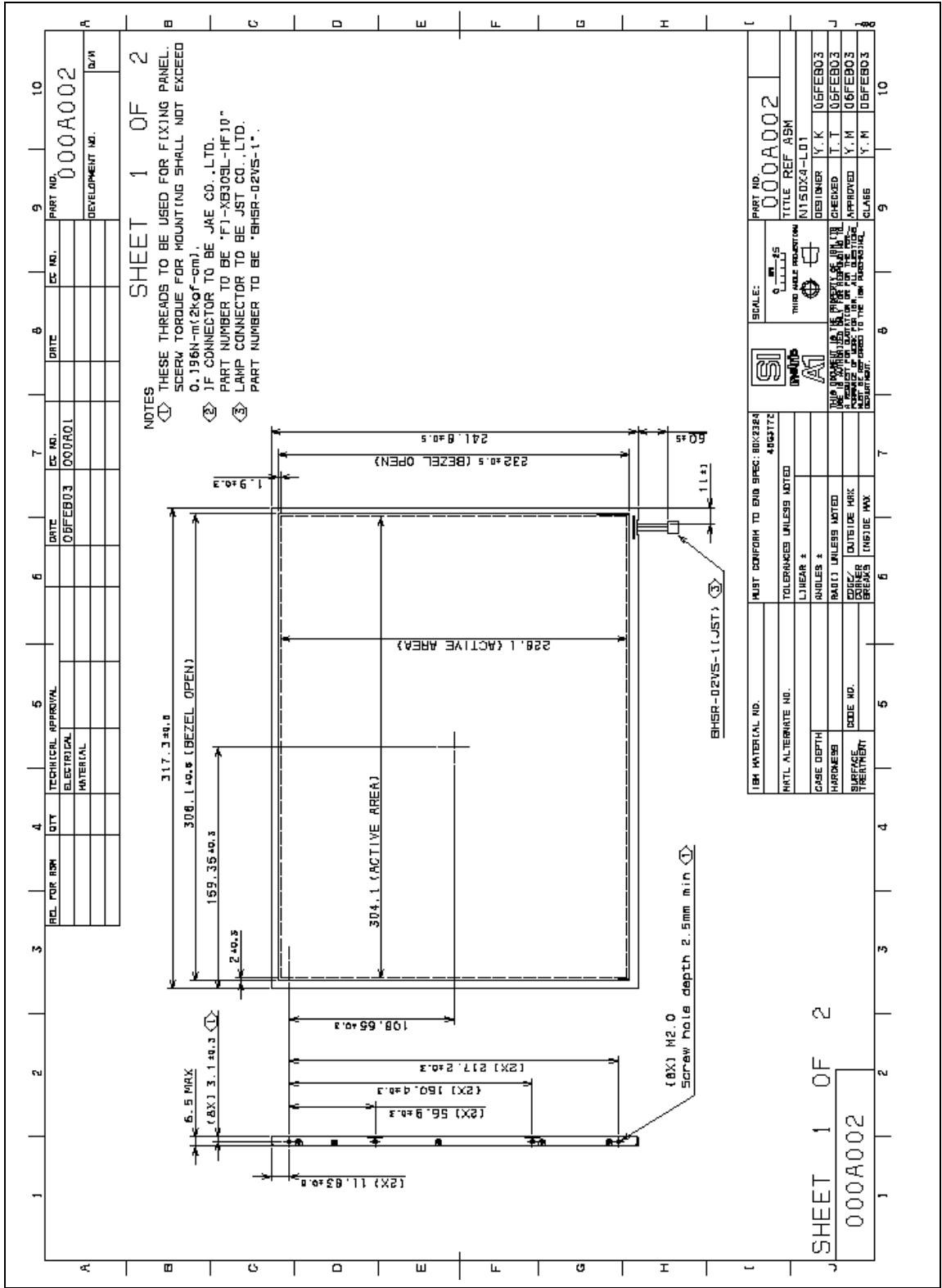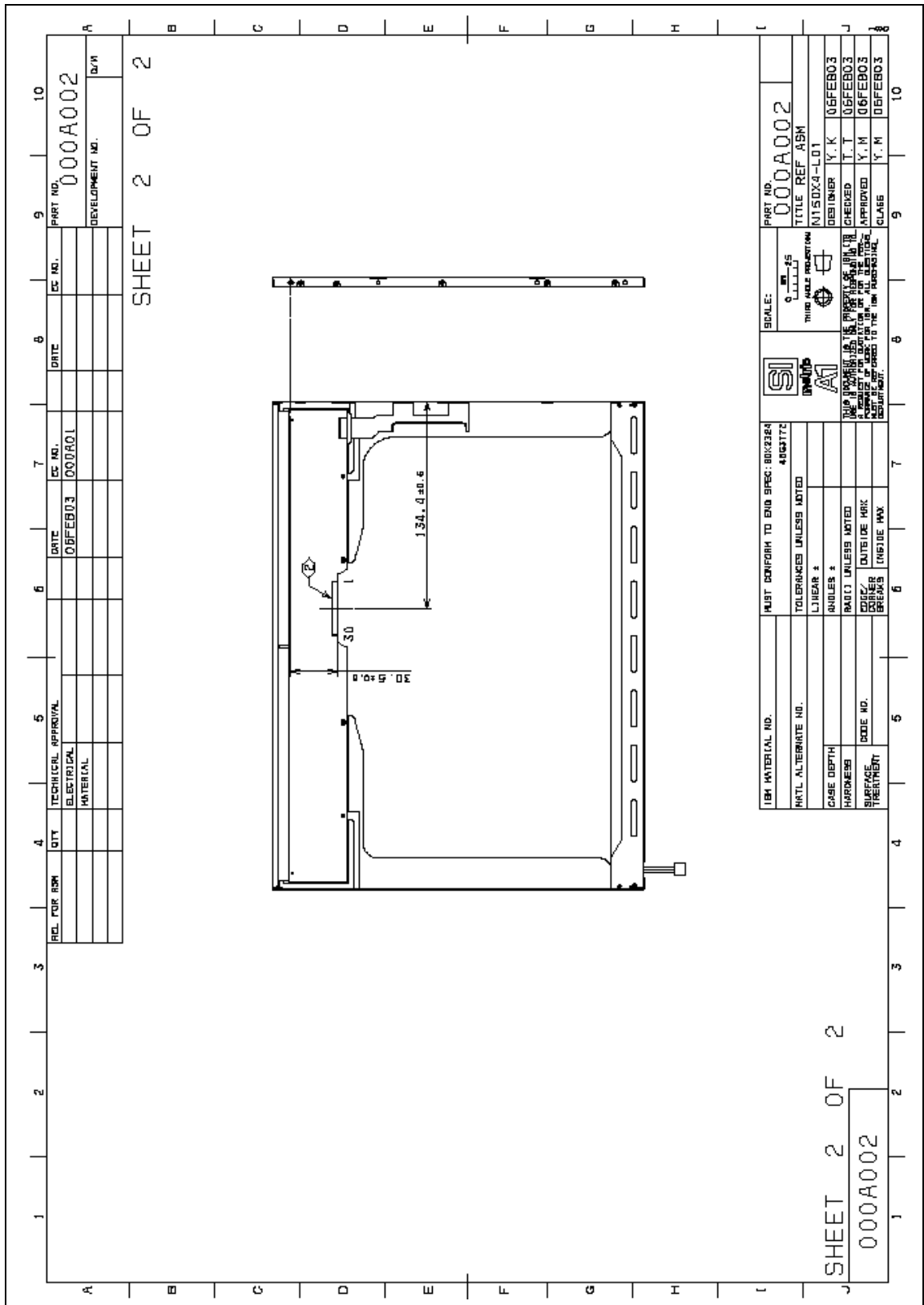
## 12.0  National Test Lab Requirement

The display module will satisfy all requirements for compliance to

UL 60950, 3rd Edition                      U.S.A. Information Technology Equipment
CAN/CSA-C22.2 No. 60950-00        Canada, Information Technology Equipment
IEC 60950 (3rd. Ed.)                        International, Information Technology Equipment
EN 60950 (3rd. Ed.)                         International, Information Technology Equipment
                                                          (European Norm for IEC60950)


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